QUASI-Z-SOURCE INVERTER BASED
PHOTOVOLTAIC POWER CONDITIONING SYSTEM

A PROJECT REPORT

Submitted by

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ABSTRACT

The quasi-Z-source inverter (QZSI) is a single stage power converter derived from the Z-source inverter topology, employing an impedance network which couples the source and the inverter to achieve voltage boost and inversion. A new carrier based pulse width modulation (PWM) strategy for the (QZSI) which gives a significantly high voltage gain compared to the traditional PWM techniques is implemented. This technique employs sine wave as both carrier and reference signal, with which the simple boost control for the shoot-through states is integrated to obtain an output voltage boost. The conventional triangular wave carrier used in simple boost control technique is replaced by sine wave, which improves the shoot-through duty ratio for a given modulation index. The conventional perturb and observe maximum power point tracking algorithm is modified for QZSI and used along with the PWM technique for tracking the maximum power from PV. All the simulations are done using MATLAB. Hardware implementation and Microcontroller programming are done in the lab.

**Keywords:** qzsi; pwm; simple boost; perturb and observe; shoot-through
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CHAPTER 1

INVERTERS

1.1 INTRODUCTION

Inverter denotes a class of power conversion circuits that operates from a DC voltage or DC current source and converts it into AC voltage or current. Static power converters are constructed from power switches and the AC output waveforms thus take discrete values. However this waveform is not sinusoidal. By employing a modulation technique that controls the time and sequence of the power switches used, the output voltage waveform obtained is more sinusoidal with less harmonic distortions. The modulating techniques mostly used are Sinusoidal pulse width modulation, space vector technique and selective harmonic elimination technique.

Inverters are classified into two types namely, Voltage source inverter (VSI) and Current source inverter (CSI).

1.2 VOLTAGE SOURCE INVERTER

The simplest voltage source for a VSI may be a battery bank which may consist of many cells in series – parallel combination. Figure 1.1 shows the power topology of a full bridge VSI. A set of large capacitor is required because the current harmonics injected by the operation of the inverter are lower order harmonics. It is clear that both the switches Q1 and Q2 cannot be on simultaneously because a short circuit across the DC link voltage source E would be produced. In order to ensure that short circuit does not occur , the modulating technique must be in such a way that either the top or the bottom switch of the inverter leg is ON.
Figure 1.1 Three phase Voltage source Inverter

Figure 1.2 depicts the conventional PWM technique. It can be seen that the output voltage will be definitely less than the input voltage. The boost operation cannot be performed as the voltage is less than the input. So VSI cannot be used for the operation of hybrid electric vehicles which require both buck and boost operation.

Figure 1.2 Sine and Triangular PWM
1.3 Z – SOURCE INVERTER

Figure 1.3 shows the general Z – source inverter. The network employs a unique impedance circuit to couple the converter main circuit to that of the power source in order to obtain the unique features that cannot be achieved using conventional VSI or CSI. The Z-source inverter (ZSI) has been reported suitable for residential PV system because of the capability of voltage boost and inversion in a single stage.

![Z-source inverter topology](image)

Figure 1.3 Z-source inverter topology

The unique feature about Z- source inverter is that the output voltage can be anywhere from zero to infinity. The inverter can perform both buck and boost operation and provide a wide range of output voltage which is not possible in conventional voltage source and current source inverters. The Z-source inverter has nine permissible switching states which has an extra state compared to the conventional inverters. The extra switching state arises from the shoot through state of the network in which two switches of the same leg is switched ON and conduct simultaneously which is not possible in conventional inverters.
CHAPTER 2

MODELLING AND SIMULATION OF PHOTOVOLTAIC MODULE

2.1 PHOTOVOLTAIC SYSTEM

Photovoltaic (PV) cells, or solar cells, take advantage of the photoelectric effect to produce electricity. PV cells are the building blocks of all PV systems because they are the devices that convert sunlight to electricity. When light falls on a PV cell, it may be reflected, absorbed, or pass right through. But only the absorbed light generates electricity. The energy of the absorbed light is transferred to electrons in the atoms of the PV cell semiconductor material. When enough photons are absorbed by the negative layer of the photovoltaic cell, electrons are freed from the negative semiconductor material. Due to the manufacturing process of the positive layer, these freed electrons naturally migrate to the positive layer creating a voltage differential, similar to a household battery.

When the 2 layers are connected to an external load, the electrons flow through the circuit creating electricity. Each individual solar energy cell produces only 1-2 watts. To increase power output, cells are combined in a weather-tight package called a solar module. These modules (from one to several thousand) are then wired up in serial and/or parallel with one another, into what's called a solar array, to create the desired voltage and amperage output required by the given project. With their newfound energy, these electrons escape from their normal positions in the atoms and become part of the electrical flow, or current, in an electrical circuit. A special electrical property of the PV cell provides the force, or voltage, needed to drive the current through an external load, such as a light bulb.
Figure 2.1 Photovoltaic effect on a solar cell

Figure 2.2 Solar Array
Multiple Solar PV modules can be wired together to form a Solar PV array. Solar PV modules and arrays produce direct current (DC) electricity. They can be connected in both series and parallel to produce any required voltage and current combination. Because a single Solar PV panel can only produce a limited amount of power, many installations contain several panels. Solar PV panels that are electrically connected together are often referred to as an array. The panels are mounted at a fixed angle facing south, or they can be mounted on a tracking device that follows the sun, allowing them to capture the most sunlight. Many solar panels combined together to create one system is called a solar array. For large electric utility or industrial applications, hundreds of solar arrays are interconnected to form a large utility-scale PV system.

### 2.2 CHARACTERISTICS OF PV MODULE

The silicon solar cell gives output voltage of around 0.7 V under open circuit condition. To get a higher output voltage many such cells are connected in series. The typical characteristic curve of a PV solar cell is shown below.

![Figure 2.3 Typical characteristic curve of a solar cell](image)

Figure 2.3 Typical characteristic curve of a solar cell
The characteristic of a PV module is non-linear which makes it difficult to determine the maximum power point. In order to extract maximum power from the PV module, it must always be operated at or very close to where the power is highest. This point is referred to as Maximum power point (MPP) and it is located around the bend or knee of the IV characteristic.

The operating characteristics of a PV panel consist of two regions: the current source region and voltage source region. As observed from the characteristic curve, in the current source region, the output current remains almost constant as the terminal voltage changes and in the voltage source region the terminal voltage varies only minimally over a wide range of output current.

The characteristics vary with solar insolation and temperature. The output power is directly proportional to the irradiance. As such, a smaller irradiance will result in reduced power output from the solar panel. However it is also observed that only the output current is affected by the irradiance. When the irradiance or light intensity is low, the flux of photon is less than when the sun is bright and the light intensity is high, thus more current is generated as the light intensity increases. The change in voltage is minimal with varying irradiance. Irradiance mainly affects the output current and the temperature mainly affects the terminal voltage.

2.3 PV MODULE EFFICIENCY FACTORS

2.3.1 Energy conversion Efficiency

Energy conversion efficiency \( \eta \), is the percentage of power converted (from absorbed light to electrical energy). When a solar cell is connected to an electrical circuit. This term is calculated using the ratio of maximum power,
\( P_m \), divided by input light irradiance (E, in W/m\(^2\)) under standard test conditions (STC) and surface area of the solar cell (A)

\[
\eta = \frac{P_m}{E \cdot A}
\]  

(2.1)

2.3.2 Maximum Power point

The load for which the cell can deliver maximum electrical power at the level of irradiation.

\[
P_m = V_{mp} \cdot I_{mp}
\]  

(2.2)

2.4 MATHEMATICAL MODELLING OF PV MODULE

2.4.1 Solar cell model

A general mathematical description of I-V output characteristics for a PV cell has been analyzed here. The equivalent circuit-based model is mainly used for the MPPT technologies. The equivalent circuit of the general model which consists of a photo current, a diode, a parallel resistor expressing a leakage current, and a series resistor describing an internal resistance to the current flow, as shown.

Figure 2.4 Simple one diode solar cell model
The voltage-current characteristic equation of a solar cell is given as

\[ I = I_{PH} - I_S \exp \left( \frac{q(V + I_{RS})}{kT_C A} - 1 \right) - \frac{(V + I_{RS})}{R_{SH}} \]  

(2.3)

Where,

- \( I_{PH} \) is a light-generated current or photocurrent,
- \( I_S \) is the cell saturation of dark current,
- \( q = 1.6 \times 10^{-19} \text{C} \) is an electron charge,
- \( k = 1.38 \times 10^{-23} \text{J/K} \) is a Boltzmann’s constant,
- \( T_C \) is the cell’s working temperature,
- \( A \) is an ideal factor,
- \( R_{SH} \) is a shunt resistance,
- \( R_S \) is a series resistance.

The generalized PV module is shown below.

Figure 2.5 Generalized PV module
The photocurrent mainly depends on the solar insolation and cell’s working temperature, which is described as

\[ I_{PH} = [I_{SC} + K_I (T_C - T_{Ref})] \lambda \]  

(2.4)

where,
- \( I_{SC} \) is the cell’s short-circuit current at a 25°C and 1kW/m²,
- \( K_I \) is the cell’s short-circuit current temperature coefficient,
- \( T_{Ref} \) is the cell’s reference temperature,
- \( \lambda \) is the solar insolation in kW/m².

On the other hand, the cell’s saturation current varies with the cell temperature, which is described as

\[ I_S = I_{RS} (T_C/T_{Ref})^3 \exp \left[ qE_G (1/T_{Ref} - 1/T_C)/kA \right] \]  

(2.5)

Where, \( I_{RS} \) is the cell’s reverse saturation current at a reference temperature and a solar radiation, \( E_G \) is the bang-gap energy of the semiconductor used in the cell.

The equivalent circuit of PV solar cell can be simplified and can be rewritten to be

\[ I = I_{PH} - I_S \left[ \exp \left( qV / kT_C A \right) - 1 \right] \]  

(2.6)
2.4.2 Solar Module and Array Model

Since a typical PV cell produces less than 2W at 0.5V approximately, the cells must be connected in series-parallel configuration on a module to produce enough high power. A PV array is a group of several PV modules which are electrically connected in series and parallel circuits to generate the required current and voltage. The equivalent circuit for the solar module arranged in NP parallel and NS series.

The terminal equation for the current and voltage of the array becomes as follows

\[ I = N_P I_{PH} - N_P I_S \left[ \exp \left( \frac{q}{N_S} \frac{V}{N_P} + I_{RS} / N_P \right) / kT \right] - \left( N_P V / N_S + I_{RS} / R_{SH} \right) \]

(2.7)

The PV efficiency is sensitive to small change in \( RS \) but insensitive to variation in \( R_{SH} \). For a PV module or array, the series resistance becomes apparently important and the shunt down resistance approaches infinity which is assumed to be open an appropriate equivalent circuit for all PV cell, module, and array is generalized.
The mathematical equation of generalized model can be described as

\[ I = N_p I_{PH} - N_p I_S \left[ \exp \left( \frac{q(V/N_S + I_{RS}/N_p)}{kT_C A} \right) - 1 \right] \]  \hspace{1cm} (2.8)

The equivalent circuit is described on the following equation

\[ I = N_p I_{PH} - N_p I_S \left[ \exp \left( \frac{qV}{N_S kT_C A} \right) - 1 \right] \]  \hspace{1cm} (2.9)

Where, \( N_S \): series number of cells for a PV array,
\( N_P \): parallel number of cells for a PV array.

2.5 MAXIMUM POWER POINT TRACKING

2.5.1 INTRODUCTION

Maximum power point tracking, frequently referred to as MPPT, is an electronic system that operates the PV modules such that the modules produce all the power they are capable of. MPPT is not a mechanical tracking system that “physically moves” the modules to make them point directly at the sun. It only varies the electrical operating point of the modules so that they deliver the maximum available power.

The following are the different MPPT methods to maximize the output power and fix its value to the highest in the steady state.

They are:

1. Perturb and observe,
2. Incremental conductance,
3. Parasitic capacitance,
4. Voltage based peak power tracking,
5. Current based peak power tracking.

2.5.2 PERTURB AND OBSERVE METHOD

The controller adjusts the voltage by a small amount from the array and measures power; if the power increases, further adjustments in that direction are tried until power no longer increases. This is called the perturb and observe method. It is also called as Hill climbing method. Perturb and observe method may result in top-level efficiency, provided that a proper predictive and adaptive hill climbing strategy is adopted. In Figure 2.7, if the operating voltage of the PV array is perturbed in a given direction and $\frac{dP}{dV} > 0$, it is known that the perturbation moved the array's operating point toward the MPP.

Figure 2.7 Sign of $\frac{dP}{dV}$ at different positions on the power characteristic.
Figure 2.8 shows the flowchart of P&O algorithm method. The P&O algorithm would then continue to perturb the PV array voltage in the same direction. If \( \frac{dP}{dV} < 0 \), change in operating point moves the PV array away from the MPP, and the P&O algorithm reverses the direction of the perturbation. The advantage of the P&O method is that it is easy to implement. However, it has some limitations, like oscillations around the MPP in steady state operation, slow response speed, and even tracking in wrong way under rapidly changing atmospheric conditions.

![Flowchart of P&O algorithm](image)

Figure 2.8 Perturb and observe algorithm
CHAPTER 3

QUASI-Z-SOURCE INVERTER

3.1 INTRODUCTION

The quasi z-source inverter (QZSI) is a single stage power converter derived from the Z-source inverter topology, employing a unique impedance network. The conventional VSI and CSI suffer from the limitation that triggering two switches in the same leg or phase leads to a source short and in addition, the maximum obtainable output voltage cannot exceed the dc input, since they are buck converters and can produce a voltage lower than the dc input voltage. Both Z-source inverters and quasi-Z-source inverters overcome these drawbacks; by utilizing several shoot-through zero states. A zero state is produced when the upper three or lower three switches are fired simultaneously to boost the output voltage. Sustaining the six permissible active switching states of a VSI, the zero states can be partially or completely replaced by the shoot through states depending upon the voltage boost requirement.

Quasi-Z-source inverters (QZSI) acquire all the advantages of traditional Z-source inverter. The impedance network couples the source and the inverter to achieve voltage boost and inversion in a single stage. By using this new topology, the inverter draws a constant current from the PV array and is capable of handling a wide input voltage range. It also features lower component ratings, reduces switching ripples to the PV panels, causes less EMI problems and reduced source stress compared to the traditional ZSI.
3.2 QZSI NETWORK

The QZSI circuit differs from that of a conventional ZSI in the LC impedance network interface between the source and inverter. The unique LC and diode network connected to the inverter bridge modify the operation of the circuit, allowing the shoot-through state which is forbidden in traditional VSI. This network will effectively protect the circuit from damage when the shoot-through occurs and by using the shoot-though state, the (quasi-) Z-source network boosts the dc-link voltage.

Figure 3.1 Quasi Z source inverter

The impedance network of QZSI is a two port network. It consists of inductors and capacitors connected as shown in fig. This network is employed to provide an impedance source, coupling the converter to the load. The dc source can be a battery, diode rectifier, thyristor converter or PV array. The QZSI topology is shown in the figure 3.1.
3.3 OPERATING PRINCIPLE AND EQUIVALENT CIRCUIT OF QZSI

The two modes of operation of a quasi z-source inverter are:

(1) Non-shoot through mode (active mode).

(2) Shoot through mode.

3.3.1 ACTIVE MODE

In the non-shoot through mode, the switching pattern for the QZSI is similar to that of a VSI. The inverter bridge, viewed from the DC side is equivalent to a current source. The input dc voltage is available as DC link voltage input to the inverter, which makes the QZSI behave similar to a VSI.

![Equivalent circuit of QZSI in Active mode](image_url)

Figure 3.2 Equivalent circuit of QZSI in Active mode

3.3.2 SHOOT THROUGH MODE.

In the shoot through mode, switches of the same phase in the inverter bridge are switched on simultaneously for a very short duration. The source however does not get short circuited when attempted to do so because of the presence LC network, while boosting the output voltage. The DC link
voltage during the shoot through states, is boosted by a boost factor, whose value depends on the shoot through duty ratio for a given modulation index.

Figure 3.3 Equivalent circuit of QZSI in Shoot through Mode

Assuming that during one switching cycle, $T$, the interval of the shootthrough state is $T_0$; the interval of non-shoot-through states is $T_1$; thus one has $T = T_0 + T_1$ and the shoot-through duty ratio, $D = T_0 / T_1$.

During the interval of the non-shoot-through states, $T_1$

\[ v_{L_1} = V_{in} - V_{C1} , \quad v_{L_2} = -V_{C2} \quad \text{(3.1)} \]

During the interval of the shoot-through states, $T_0$,

\[ v_{L_1} = V_{C2} + V_{in} , \quad v_{L_2} = V_{C1} \quad \text{(3.2)} \]

\[ v_{PN} = 0 , \quad v_{\text{diode}} = V_{C1} + V_{C2} \quad \text{(3.3)} \]

At steady state, the average voltage of the inductors over one switching cycle is zero.

\[ V_{PN} = V_{C1} - v_{L_2} = V_{C1} + V_{C2} , \quad v_{\text{diode}} = 0 \quad \text{(3.4)} \]
From (3.1) and (3.3),

\[
\{ V_{L1} = v_{L1} = \frac{T_0(v_{C2} + v_{in}) + T_1(v_{in} - v_{C1})}{T} = 0 \tag{3.5} \]
\[
\{ V_{L2} = v_{L2} = \frac{T_0(v_{C1}) + T_1(-v_{C2})}{T} = 0 \tag{3.6} \]

Thus,

\[
V_{c1} = \frac{T_1}{T_1 - T_0} V_{in} \quad V_{C2} = \frac{T_0}{T_1 - T_0} V_{in} \tag{3.7} \]

From (3.4), (3.6) and (3.7), the peak dc-link voltage across the inverter bridge is

\[
v_PN = V_{c1} + V_{C2} = \frac{T}{T_1 - T_0} V_{in} = \frac{1}{1 - 2\frac{T_0}{T}} V_{in} = BV_{in} \tag{3.8} \]

where \( B \) is the boost factor of the QZSI. This is also the peak voltage across the diode.

The average current of the inductors \( L1, L2 \) can be calculated by the system power rating \( P \)

\[
I_{L1} = I_{L2} = I_{in} = \frac{P}{V_{in}} \tag{3.9} \]

According to Kirchhoff’s current law and (3.9), we also can get that

\[
I_{c1} = I_{c2} = I_{PN} - I_{L1} \quad I_D = 2I_{L1} - I_{PN} \tag{3.10} \]

Hence QZSI inherits all the advantages of the ZSI. It can buck or boost a voltage with a given boost factor. It is able to handle a shoot through state, and therefore it is more reliable than the traditional VSI. It is unnecessary to add a dead band into control schemes, which reduces the output distortion. In addition, there are some unique merits of the QZSI when compared to the ZSI.
3.4 DESIGN OF IMPEDANCE NETWORK

3.4.1 INDUCTOR DESIGN

During traditional operation mode, the capacitor voltage is always equal to the input voltage. So there is no voltage across the inductor. During shoot-through mode, the inductor current increases linearly and the voltage across the inductor is equal to the voltage across the capacitor.

The average current through the inductor is given by,

\[ I_L = \frac{P}{V_{dc}} \quad (3.11) \]

Where \( P \) is the total power and \( V_{dc} \) is the input voltage.

The average current at 1kW and 150 V input is

\[ I_L (\text{avg}) = \frac{1000}{150} = 6.67 \text{A} \]

The maximum current occurs through the inductor when the maximum shoot-through happens, which causes maximum ripple current. In this design, 30% current ripple through the inductors during maximum power operation was chosen. Therefore the allowed ripple current was 4A and maximum current is 10.67A.

For a switching frequency of 10 kHz, the average capacitor voltage is

\[ V_C = \frac{(1-T_O/T) \ast V_{dc}}{(1-2T_O/T)} \quad (3.12) \]

Substituting the values in the above equation 3.2 the average capacitor voltage is 300V. So the inductance must be no less than

\[ L = 0.1 \ast 10 \ast 300 / 10.67 = 3 \text{mH} \]
3.4.2 CAPACITOR DESIGN

The purpose of the capacitor is to absorb the voltage ripple and maintain a fairly constant voltage. During shoot-through the capacitor charges the inductors and the current through the capacitor equals the current in the inductor. Therefore the voltage ripple across the capacitor is

\[ V_C = \frac{I_{L(avg)} T_s}{C} \]  

(3.13)

The capacitor voltage ripple is 0.17%.

Substituting the above values in the equation the required capacitance was found to be

\[ C = 6.67 \times 0.1 \times 10 (300 \times 0.0017) = 1000 \mu F \]

Hence the impedance network of the Quasi Z-Source inverter consists of a inductor of value 3mH and capacitor of 1000\mu F.
CHAPTER 4

PWM CONTROL STRATEGY

4.1 INTRODUCTION

The QZSI configuration has six active vectors when the DC voltage is impressed across the load and two zero vectors when the load terminals are shorted through either lower or upper three switches. These total eight switching states and their combinations have been spawned many PWM control schemes. Sinusoidal PWM is the most commonly used PWM technique in the VSI. On the other hand, QZSI has additional zero vectors or shoot through switching states that are forbidden in traditional VSI. For an output voltage boost to be obtained, a shoot through state should always be followed by active state. Three phase inverter must be controlled so that at no time both the switches in the same leg are turned on or else the DC supply would be shorted. This requirement may be met by the complimentary operations of the switches within a leg. There are three PWM strategies

1. Simple boost control

2. Maximum Boost control

3. Maximum constant boost control.

We have adopted Simple boost control technique.

4.2 COMPARISON OF SINE AND TRIANGULAR PWM

A PWM control technique for QZSI, with modified carrier for active and shoot through states is presented. While the zero states of traditional VSI are replaced
by shoot through states, the active states should remain unaltered, for the shape
of output voltage waveform to be preserved. This technique uses sine wave as
both reference and carrier. The simple boost control method used here employs
two constant voltage envelopes which are compared with the sine carrier wave.
Whenever the magnitude of sine carrier wave becomes greater than or equal to
the positive constant magnitude envelope (or) lesser than or equal to the negative
constant magnitude envelope, pulses are generated and they control the shoot
through duty ratio $D_o$. These pulses serves as firing signals for the switches in the
inverter. Figure 4.1 illustrates the arrangement of sine carrier PWM. Table 4.1
illustrates the comparison of sine and triangular PWM

4.3 OPERATION OF SINE PWM

![Schematic of Sine PWM](image)

Figure 4.1 Schematic of Sine PWM
Therefore the voltage gain $G$ of QZSI is given by,

$$\frac{\text{Output peak AC voltage}}{\text{DC link voltage}} = G$$  \hspace{1cm} (4.1)

$$V_{\text{link}} = \frac{V_s}{2}$$  \hspace{1cm} (4.2)

$$V_{\text{ac}} = MB \times \frac{V_s}{2}$$  \hspace{1cm} (4.3)

Where $V_{\text{link}}$ is the DC link voltage of inverter

$V_{\text{ac}}$ is the peak ac output voltage

$B$ is the boost factor

$M$ is modulation index

The boost factor is given by,

$$B = \frac{T}{T_1 - T_0} = \frac{1}{1 - 2 \frac{T_0}{T}} = \frac{1}{1 - 2D_0}$$  \hspace{1cm} (4.4)

where $D_o$ is the shoot through duty ratio of QZSI, $T_o$ is the shoot through interval, $T$ is the switching cycle.

When a triangular carrier is employed, the shoot through duty ratio, boost factor and voltage gain are given as

$$D_o = 1 - M$$  \hspace{1cm} (4.5)

$$B = \frac{1}{2M - 1}$$  \hspace{1cm} (4.6)
\[ G = \frac{M}{2M - 1} \]  \hspace{1cm} (4.7)

It can be seen that improvement in duty ratio can be achieved only by reduction in M, which limits the gain and leads to more voltage stress on the switch. By implementing sine carrier PWM, the shoot through ratio, the boost factor and voltage gain of QZSI are derived as

\[ D_o = \frac{T_0}{T} = 1 - \frac{2}{\pi} \sin^{-1} M \]  \hspace{1cm} (4.8)

\[ B = \frac{\pi}{4 \sin^{-1} M - \pi} \]  \hspace{1cm} (4.9)

\[ G = \frac{\pi M}{4 \sin^{-1} M - \pi} \]  \hspace{1cm} (4.10)

It is observed that sine carrier PWM gives high shoot through duty ratio compared to triangular carrier, for the same modulation index, which reduces the voltage stress on the device and gives high peak output voltage. The simple boost control method has shoot through states spread uniformly which makes output free of low frequency ripples. The use of sine carrier wave has also resulted in reduction of THD in output voltage, improved fundamental component.
CHAPTER 5

SIMULATION RESULTS

5.1 PHOTOVOLTAIC SYSTEM

The PV array module is implemented using a generalized photovoltaic model using MATLAB Simulink software package. The effect of solar irradiation cell temperature, output current and power characteristics of PV module are simulated, analyzed and optimized. A simple mathematical relation is used to model the non-linear characteristics of solar cell. The solar irradiation level is controlled by varying the short circuit current in the characteristic equation. From the characteristics the maximum power point is calculated. The simulation of solar cell is performed using the MATLAB software and I-V and P-V Characteristics are obtained.

5.1.1 PV CELL MODEL

![Figure 5.1 PV cell model](image)
5.1.2 PV MODEL CHARACTERISTICS

**FOR DIFFERENT INSOLATIONS, \( \lambda \) (WATTS/M\(^2\))**

**FOR DIFFERENT TEMPERATURE INPUTS, \( T \)**

Figure 5.2 Characteristics of PV cell
5.2 QUASI Z- SOURCE INVERTER

Figure 5.3 Quasi Z source inverter model
5.2.1 OUTPUT LINE VOLTAGE AND CURRENT

Figure 5.4 Output current and voltage waveforms

5.2.2 COMPARISON OF SINE AND TRIANGULAR PWM

A PWM control technique for QZSI, with modified carrier for active and shoot through states is presented. While the zero states of traditional VSI are replaced by shoot through states, the active states should remain unaltered, for the shape of output voltage waveform to be preserved. This technique uses sine wave as both reference and carrier. The simple boost control method used here employs two constant voltage envelopes which are compared with the sine carrier wave. Whenever the magnitude of sine
carrier wave becomes greater than or equal to the positive constant magnitude envelope (or) lesser than or equal to the negative constant magnitude envelope, pulses are generated and they control the shoot through duty ratio Do.

Table 5.1 Comparison of Sine and triangular PWM (For G =2.88)

<table>
<thead>
<tr>
<th>Harmonic Component</th>
<th>Triangular Carrier PWM</th>
<th>Sine Carrier PWM</th>
</tr>
</thead>
<tbody>
<tr>
<td>h3</td>
<td>0.02</td>
<td>0.07</td>
</tr>
<tr>
<td>h5</td>
<td>7.61</td>
<td>1.09</td>
</tr>
<tr>
<td>h7</td>
<td>3.28</td>
<td>0.3</td>
</tr>
<tr>
<td>h9</td>
<td>0.16</td>
<td>0.02</td>
</tr>
<tr>
<td>h11</td>
<td>8.29</td>
<td>0.15</td>
</tr>
<tr>
<td>h13</td>
<td>0.02</td>
<td>0.07</td>
</tr>
<tr>
<td>h15</td>
<td>0.05</td>
<td>0.03</td>
</tr>
<tr>
<td>h17</td>
<td>2.02</td>
<td>0.06</td>
</tr>
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<td>h19</td>
<td>5.93</td>
<td>0.07</td>
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<td>1.34</td>
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<tr>
<td>h27</td>
<td>0.07</td>
<td>0.03</td>
</tr>
<tr>
<td>h29</td>
<td>3.85</td>
<td>0.06</td>
</tr>
<tr>
<td>THD</td>
<td>6.722</td>
<td>1.163</td>
</tr>
</tbody>
</table>
5.2.3 THD WAVEFORMS FOR LINE VOLTAGE AND CURRENT

![Figure 5.5 Frequency spectrum of line voltage](image1)

*Fundamental (50Hz) = 36.66, THD = 1.16%*

![Figure 5.6 Frequency spectrum of line current](image2)

*Fundamental (50Hz) = 0.5325, THD = 1.09%*

Figure 5.5 Frequency spectrum of line voltage

Figure 5.6 Frequency spectrum of line current
CHAPTER 6
GENERATION OF PWM PULSES THROUGH PIC

6.1 INTRODUCTION

The PIC18F4550 microprocessor manufactured by Texas instruments is a high performance, highly integrated processor used as a controller for the inverter circuit.

The PIC18F4550 has a C Compiler Optimized Architecture with Optional Extended Instruction Set. It consists of 100,000 Erase/Write Cycle Enhanced Flash and its program memory is typical one. Flexible oscillator option is available in this PIC18F4550. It includes Four Crystal modes, including High-Precision PLL for USB. It has two External Clock modes, Up to 48 MHz. The Internal Oscillator consists of 8 user-selectable frequencies, from 31 kHz to 8 MHz Dual Oscillator Options allow Microcontroller and USB module to run at different Clock Speeds.

6.2 PERIPHERALS

The **PIC18F4550 microcontroller** consists of following peripherals:

6.2.1 I/O Ports

PIC18F4550 have 5 (PORTA, PORTB, PORTC, PORTD and PORTE) 8-bit input-output ports. PORTB &PORTD have 8 I/O pins each. Although other three ports are 8-bit ports but they do not have eight I/O pins. Although the 8-bit input and output are given to these ports, but the pins which do not exist, are masked internally.
6.2.2 Memory

PIC18F4550 consists of three different memory sections:

1. **Flash Memory**: Flash memory is used to store the program downloaded by a user on to the microcontroller. Flash memory is non-volatile, i.e., it retains the program even after the power is cut-off. PIC18F4550 has 32KB of Flash Memory.

2. **EEPROM**: This is also a nonvolatile memory which is used to store data like values of certain variables. PIC18F4550 has 256 Bytes of EEPROM.

3. **SRAM**: Static Random Access Memory is the volatile memory of the microcontroller, i.e., it loses its data as soon as the power is cut off. PIC18F4550 is equipped with 2 KB of internal SRAM.

6.2.3 Oscillator

The PIC18F series has flexible clock options. An external clock of up to 48 MHz can be applied to this series. These controllers also consist of an internal oscillator which provides eight selectable frequency options varying from 31 kHz to 8 MHz.

6.2.4 8x8 Multiplier

The PIC18F4550 includes an 8 x 8 multiplier hardware. This hardware performs the multiplications in single machine cycle. This gives higher computational throughput and reduces operation cycle & code length.
6.2.5 ADC Interface
PIC18F4550 is equipped with 13 ADC (Analog to Digital Converter) channels of 10-bits resolution. ADC reads the analog input, for example, a sensor input and converts it into digital value that can be understood by the microcontroller.

6.2.6 Timers/Counters
PIC18F4550 has four timer/counters. There is one 8-bit timer and the remaining timers have option to select 8 or 16 bit mode. Timers are useful for generating precision actions, for example, creating precise time delays between two operations.

6.2.7 Interrupts
PIC18F4550 consists of three external interrupts sources. There are 20 internal interrupts which are associated with different peripherals like USART, ADC, Timers, and so on.

6.2.8 EUSART
Enhanced USART (Universal Synchronous and Asynchronous Serial Receiver and Transmitter) module is full-duplex asynchronous system. It can also be configured as half-duplex synchronous system. The Enhanced USART has the feature for automatic baud rate detection and calibration, automatic wake-up on Sync Break reception and 12-bit Break character transmit. These features make it ideally suited for use in Local Interconnect Network bus (LIN bus) systems.
6.2.9 ICSP and ICD

PIC18F series controllers have In Circuit Serial Programming facility to program the Flash Memory which can be programmed without removing the IC from the circuit. ICD (In Circuit Debugger) allows for hardware debugging of the controller while it is in the application circuit.

6.2.10 SPI

PIC18F supports 3-wire SPI communication between two devices on a common clock source. The data rate of SPI is more than that of USART.

6.2.11 \(I^2C\)

PIC18F supports Two Wire Interface (TWI) or \(I^2C\) communication between two devices. It can work as both Master and Slave device.

6.2.12 USB

PIC18F supports full-speed USB with different clock options.

6.3 FEATURES OF PIC 18F4550

![Figure 6.2 pin configuration of 18f4550](image)
- High current sink/source 25mA/25 mA
- Three External interrupts
- Enhanced capture/compare /PWM (ECCP) module
- Compatible 10 bit , up to 13 channels ADC module
- Captures 16 bit , maximum resolution is 6.25 ns
- Compares 16 bit , maximum resolution is 100 ns
- 8 * 8 single cycle hardware multiplier
- 100,000 erase / write cycle Enhances FLASH program memory
- 1,000,000 erase/write cycle Data EEPROM memory
- 8 user selectable frequencies
- Two external clock modes , up to 48 MHz

6.4 FUNCTIONAL BLOCK DIAGRAM

Figure 6.1 Functional Block diagram
6.5 PROGRAMMING IN PIC

The programming has been done in MPLAB using its C18 compiler. The program code is done in C and saved in a (.C) file. The header files (p18f4550.h and delays.h) and library file (p18f4550.lib) and linker file (18f4550.lkr) are included. The source file is a (.C) file and the workspace is stored as a (.mcw) file. The source code is built using pickit2 and the source code is loaded in the PIC for generating pulses.
CHAPTER 7
HARDWARE IMPLEMENTATION

7.1 INTRODUCTION

The hardware of Z-source inverters contains the impedance network, pic kit for generating firing pulses, isolation circuit, the power circuit and the load.

7.2 IMPEDANCE NETWORK

The quasi Z-source inverter consists of an impedance network connected between the DC voltage source and the conventional VSI. A symmetrical impedance network consists of two identical capacitors and inductors connected as shown in the figure 7.1. By connecting in this manner the inverter can be operated in shoot-through. The diode is necessary for preventing the discharge of capacitors through the input source. The values of inductor and capacitor for the impedance network are determined already in Chapter 3.

Figure 7.1 Impedance network
The ratings of inductors and capacitors used in the hardware are mentioned below

Capacitors $C_1, C_2 = 1000\mu F, 450V$

Inductors $L_1, L_2 = 3mH, 5A$

Diode = IN5408(3A, 700V)

### 7.3 INVERTER CIRCUIT

The inverter circuit of the QZSI is similar to that of a conventional three phase VSI. The power circuit which follows the impedance network consists of 6 IGBT switches. 2 IGBTs are arranged in each arm such that emitter of the first IGBT is connected to the collector of the second IGBT. The emitter-collector junction of each arm is then connected to the three phase load. PWM pulses that are obtained from the Digital signal processor are given to the gate of the IGBTs through the isolation circuit.

The IGBTs, FGA25N120ANTD manufactured by Fairchild semiconductor have a rating of 1200V and 25A under normal operating conditions.

![Figure 7.2 Inverter circuit](image-url)
7.4 ISOLATION CIRCUIT

The isolation circuit offers isolation between the power circuit and the Digital signal Processor which generates the PWM pulses. It is required because the eZdsp board is sensitive and operates at very low voltage levels. The optocouplers also protect the Digital signal Processor from any reverse currents flowing from the inverter power circuit. Figure 7.3 shows the circuit diagram of optocouplers.

![Figure 7.3 MCT2E optocoupler](image)

The isolation is provided by 6 MCT2E optocouplers, each for one IGBT. The optocouplers circuit implemented in DOT board is shown in figure 7.4.

7.5 OPTOCOUPLER SUPPLY CIRCUIT

The supply for the isolator circuit is obtained from the power supply. The AC supply is first stepped down using a transformer and then it is rectified into DC using Diode bridge rectifiers. The bridge rectifier is followed by voltage regulator IC and filter circuits to smoothen out the DC voltage obtained from
the outputs of the diode bridge rectifier. The ratings of the components used in the bridge circuit are indicated below.

Transformer: 0-18 V

Bridge rectifier: W10M

Voltage regulator: LM7818, 18V

Filter capacitor: 100µF, 63V

Figure 7.4 Optocoupler circuit
CHAPTER 8
CONCLUSION

8.1 CONCLUSION

PV array has been simulated and integrated to the QZSI with maximum power point tracking algorithm (perturb and observe method). QZSI has been simulated with sine carrier and triangular carrier and the results have been compared and the individual harmonic contributions have been analyzed. The proposed QZSI inherits all the advantages of the ZSI and features its unique merits. It can realize buck/boost power conversion in a single stage with a wide range of gain that is suited well for application in PV power generation systems. Furthermore, the proposed QZSI has advantages of continuous input current, reduced source stress, and lower component ratings when compared to the traditional ZSI. The voltage gain with sine carrier is greater than the voltage gain with triangular carrier. The hardware implementation of power and control circuits has been implemented. Switching pulses are generated using PIC18f4550.

8.2 SCOPE FOR FUTURE WORK

A grid-connected PV power generation system is one of the most promising applications of renewable energy sources. The proposed QZSI based PV power generation system is intended as a grid connected system and transfers the maximum power from the PV array to the grid by maximum power point tracking technology. QZSI is best suited interface for photovoltaic power generation system and could prove to be highly efficient, when implemented with the improved control techniques proposed.
APPENDIX 1

PIC PROGRAM

#include<p18f4550.h>
#include<delays.h>

#pragma config FOSC = INTOSCIO_EC,FCMEN = OFF,IESO = OFF,PWRT =
OFF,BOR = OFF,WDT = OFF,LVP = OFF,MCLRE = OFF,STVREN = OFF,CP0
= OFF,CP1 = OFF,CP2 = OFF,CP3 = OFF,CPB = OFF,CPD = OFF,WRT0 =
OFF,WRT1 = OFF,WRT2 = OFF,WRT3 = OFF,WRTC = OFF,WRTB =
OFF,WRTD = OFF,EBTR0 = OFF,EBTR1 = OFF,EBTR2 = OFF,EBTR3 =
OFF,EBTRB = OFF

void main(void)
{
    TRISB=0x00;
    OSCCON=0x77;
    while(1)
    {
        LATB=0x85;
        Delay10TCYx(23);
        Delay1TCY();
        LATB=0xAF;
Delay10TCYx(30);
Delay1TCY();
Delay1TCY();
Delay1TCY();
LATB=0x85;
Delay10TCYx(46);
LATB=0xAC;
Delay10TCYx(50);
LATB=0xA8;
Delay10TCYx(18);
Delay1TCY();
Delay1TCY();
Delay1TCY();
LATB=0xAF;
Delay10TCYx(31);
LATB=0xA8;
Delay10TCYx(46);
LATB=0xAC;
Delay10TCYx(35);
Delay1TCY();
Delay1TCY();
LATB=0x85;
Delay10TCYx(9);
LATB=0xAF;
Delay10TCYx(10);
LATB=0x85;
Delay10TCYx(40);
Delay1TCY();
Delay1TCY();
Delay1TCY();
Delay1TCY();
Delay1TCY();
Delay1TCY();
LATB=0xAC;
Delay10TCYx(12);
LATB=0xA8;
Delay10TCYx(3);
Delay1TCY();
Delay1TCY();
LATB=0xAF;
Delay10TCYx(38);
Delay1TCY();
Delay1TCY();
Delay1TCY();
LATB=0xA8;
Delay10TCYx(46);
LATB=0xA1;
Delay10TCYx(37);
Delay1TCY();
LATB=0x85;
Delay10TCYx(6);
LATB=0xAF;
Delay10TCYx(1);
LATB=0x85;
Delay10TCYx(46);
LATB=0xA1;
Delay1TCY();
Delay1TCY();
Delay1TCY();
Delay1TCY();
Delay1TCY();
Delay1TCY();
Delay1TCY();
Delay1TCY();
Delay1TCY();
Delay1TCY();
Delay1TCY();
 Delay1TCY();
 LATB=0xA8;
 Delay10TCYx(11);
 Delay1TCY();
 Delay1TCY();
 Delay1TCY();
 Delay1TCY();
 Delay1TCY();
 Delay1TCY();
 Delay1TCY();
 LATB=0xAF; } }
APPENDIX 2

REFERENCES


